EXPERIMENTAL PULSE GENERATOR FOR STUDYING THE ELEMENTARY EDM PROCESS

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ABSTRACT

Based on a previous study pointing out the opportunity to adjust certain parameters of electric pulses in EDM, the paper presents a pulse generator structure with several new possibilities to modify work parameters. The principle of the pulse generator is described and an implement solution using a complex programmable logic device (CPLD) is presented.

KEYWORDS : EDM, generator, VHDL, CPLD

1. GENERAL STRUCTURE

The general design of this pulse generator is based on previous studies emphasizing the electric pulse parameters that have to bee controlled in order to influence the erosion speed in EDM [1,2]. This new design comes to enlarge the investigation possibilities of an experimental pulse generator [4,5], previously realized at the Non Conventional Technologies Research Center of the "Lucian Blaga" University of Sibiu.

The pulse generator (Fig.1) uses a 20 A static power switch [4,5] driven by a digital control unit, able to modify two of the pulse parameters : the space factor (η) and the number of pulses (a) in a programmed train [3].

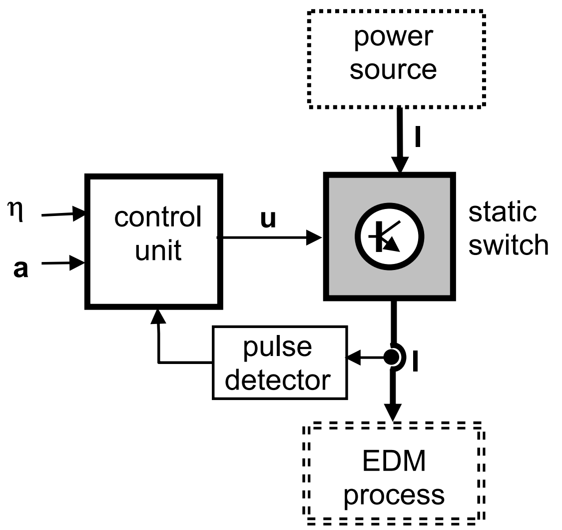

Fig.1 General structure of the generator

2. MODIFIABLE η SPACE FACTOR UNIT

The timing parameters of the command signal **u** are presented in Fig.2.

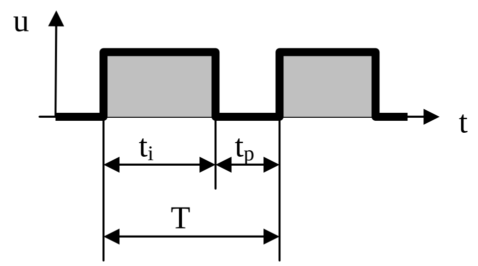

Fig.2 Timing parameters of the command signal

The space factor is :

$$\eta = \frac{t_i}{t_i + t_p} = \frac{t_i}{T} = t_i \cdot f \qquad (1)$$

where :

ti : the pulse duration [s],
tp : the pause duration [s],
T : the cycle duration (period) [s],
f : the signal frequency [Hz].

The waveform of **u**, having the frequency f, is defined using a pilot signal $\mathbf{u_o}$, having the period T_o << T, that means the frequency f_o >> f. The durations t_i, t_p are measured in number of pilot pulses $\mathbf{n_i}$, respectively $\mathbf{n_p}$, as shown in Fig.3.

The pulse duration is :

$$t_i = n_i \cdot T_o = \frac{n_i}{f_o} \qquad (2)$$

Equations (1) and (2) let to express the space factor in function of the number **n_i** of pilot pulses and the frequency ratio :

$$\eta = n_i \cdot \frac{f}{f_o} \qquad (3)$$

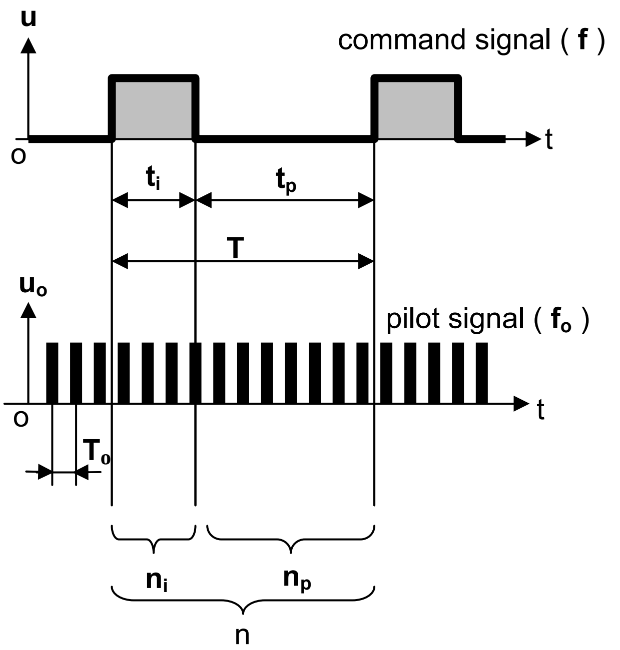

Fig.3 Defineing the command signal u by a pilot signal u_o

Equation (3) suggests the possibility to modify the space factor independently of the signal frequency f, by maintaining the ratio f/f_o constant. The numbers of pilot pulses n_i and n_p required to realize a given value η of the command signal are as follows :

$$n_i = \eta \cdot \frac{f_o}{f} \qquad (4)$$

$$n_p = n - n_i = \frac{T}{T_o} - n_i = \frac{f_o}{f} - n_i \qquad (5)$$

In this case, the space factor η can be controlled only by the number n_i of pilot pulses and the frequency ratio f_o/f.

This principle can be implemented by a digital block structured as shown in Fig.4. The pilot f_o frequency is supplied by an external timing circuit. The f_o/f ratio and the number of pulses n_i are applied in digital form, using each a k bits word. An arithmetic block calculates the number of pulses n_p in accordance with equation (5). A selector (k-bit multiplexer) delivers successively n_i and n_p to a comparator. This one compares the n_i or n_p value to the number **x** of pilot pulses,

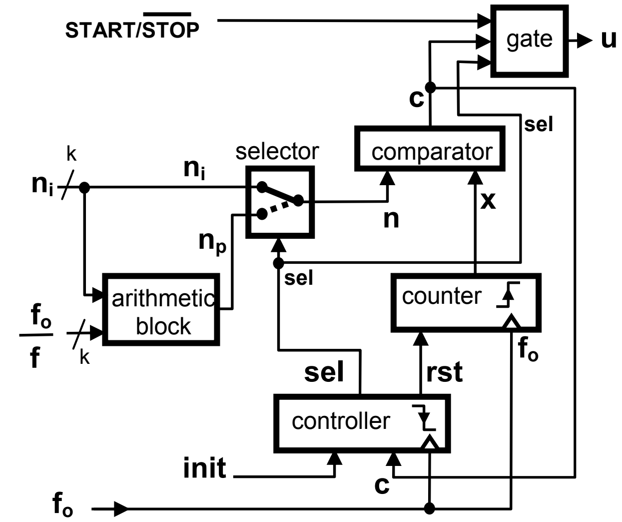

Fig.4 Principal of the space factor block

delivered by a counter. When the two values are equal the comparator delivers the c bit acting on a gate. This gate delivers the command signal **u** to the static power switch. The gate is opened if **sel** shows that the counter is operating in the pulse interval t_i. If **sel** shows that the counter is operating in the pause interval t_p the gate is closed. The output bit **c** of the comparator acts on a controller who recycles the counter each time that t_i or t_p where defined. The SART/STOP signal of the device acts on the same output gate.

Fig.5 presents the internal structure of the arithmetic block.

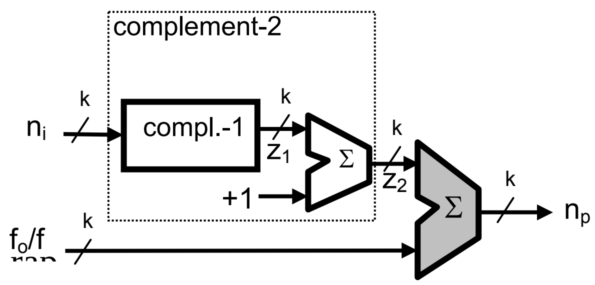

Fig.5 Structure of the arithmetic block

The arithmetic block consists of a complement-2 logic and a k-bit adder, calculating $n_p = f_o/f - n_i$. The complement-2 is calculated by incrementing with 1 the result of a complement-1 circuit.

The operation of the space factor block is dictated by a local controller. The state diagram of this controller is presented in Fig.6. The **init** external signal brings the controller in the S3 state. In this state the counter is recycled by the **rst** bit. At a **START** command the controller begins to operate in S_0 state. The selector applies $\mathbf{n_i}$ at the comparator input and the counter begins to run. The S_0 state is maintained until the comparator delivers **c** = 1, commanding the transition in S_1. In this state the counter is

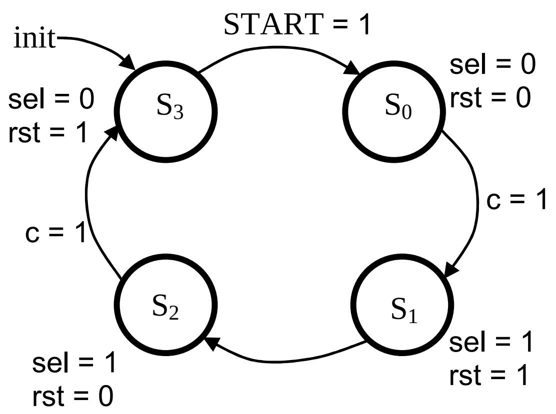

Fig.6 State diagram of the local controller

recycled and the selector is switched to apply $\mathbf{n_p}$ to the comparator. In state S_2 the counter is counting again, until the comparator output becomes **c** = 1. This event brings the controller in the initial state S_3. The cycle is repeated wile the START command is maintained on 1.

The definition $\Delta\eta$ of the space factor η is dependent of the amount of f_o/f ratio, that is of the number of bits k used to represent n_i and f_o/f. Table 1 shows this dependence.

Table 1. Dependence of the space factor definition of f_o/f and k

Frequency ratio f_o/f	No.of bits k	Definition of the space factor $\Delta\eta$%
200	8	0.5%
100	7	1%
50	6	2%
20	5	5%
10	4	10%

In usual applications the last case in Table 1 is to prefer, a definition of 10% being satisfactory. In this case the ratio f_o/f = 10, that means that the f frequency of the command signal **u** will be 10 times lower as the pilot frequency f_o and the number of pulses n_i will represent the space factor η multiplied by 10. In the present application a number of k = 5 bits has be chosen, in order to improve the space factor definition to 5%.

3. MODIFIABLE PULSE NUMBER UNIT

A circuit designed to modify the pulse number **a** of a pulse train was presented in [3]. It has been conceived for experimental studies regarding the effect of successive discharges in EDM. The block diagram of this unit is shown in Fig.7.

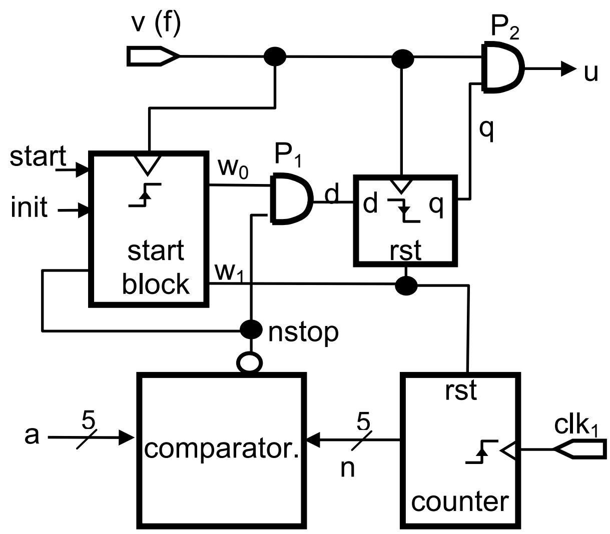

Fig.7 Modifiable pulse number unit

4. THE COMPLETE CONTROL UNIT

The architecture of the control unit, containing the two previous presented blocks, is shown in Fig.9. START 1 is a general on/off signal and START 2 releases the programmed pulse train.

5. SIMULATION AND IMPLEMENT

Fig.8 presents an example of simulation result : the control unit delivers a train of a=9 pulses with a space factor η=0,3.

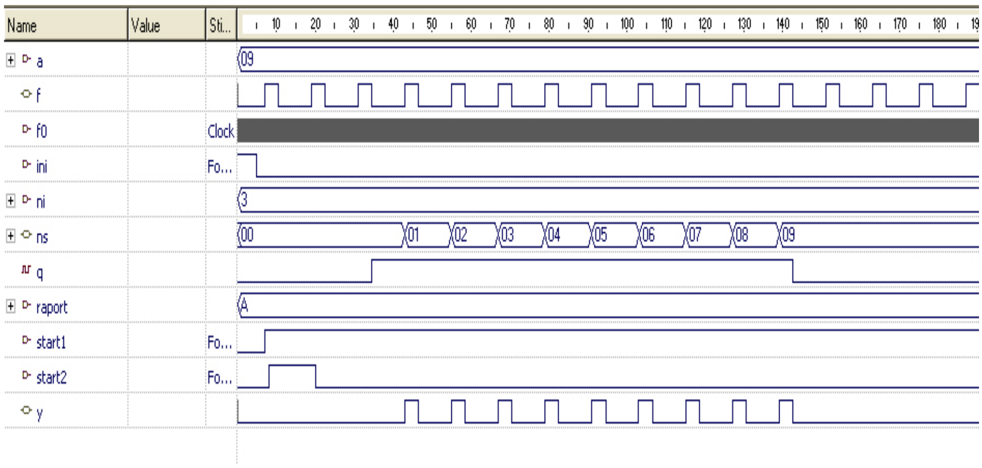

Fig 8 Simulation result

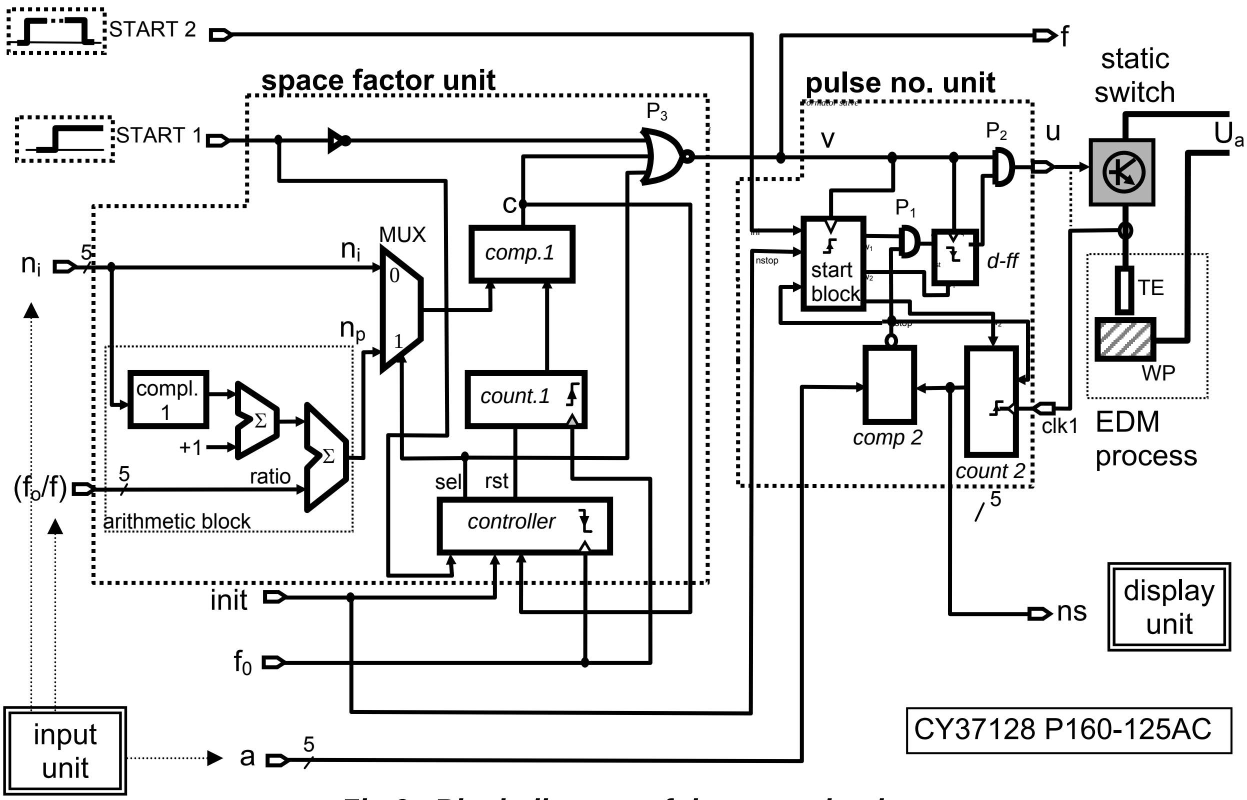

Fig.9 Block diagram of the control unit

The project was elaborated using VHDL and WARP-5.1 as development tool [3].The simulation tool was ALDEC-ActivHDLSim3.3. The target circuit was CY37128 P160, a medium size CPLD made by Cypress.

6. CONCLUSION

The described pulse generator offers the possibility to study the influence of frequency, space factor and number of repetitive pulses on the EDM elementary process. Using programmable circuits and VHDL design techniques it becomes relatively easy to realize a variety of control units, with a large capability of modifying pulse parameters.

REFERENCES

[1] NANU, D., DIACONESCU,C., ȚÎȚU, M., A Theoretical Study About the Influence of

Pulse Parameters on the Dynamics of the EDM Process, ICNcT, Bucuresti,2005
[2] NANU, D., DIACONESCU,C., ȚÎȚU, M., A Fuzzy Model of the Active Gap in EDM, ICNcT, Iaşi, 2007
[3] DIACONESCU,C., NANU, D ,ȚÎȚU, M., Implement with Programmable Logic Devices of the Control Unit of a Pulse Generator for Experimental Studies in EDM, ICNcT, Bucuresti,2005
[4] DIACONESCU, C., NANU, D., OPREAN, C., ȚÎȚU M., Echipament pentru generarea unor impulsuri pentru prelucrarea prin eroziune electrică, The IV-th Conference on New Technologies and Design Methods in Mechanical Engineering, CRAIOVA, 1998
[5] ȚÎȚU, M., NANU, D., OPREAN, C., DIACONESCU, C., ȚÎȚU, G. A., Echipament electronic pentru generarea unor descarcari singulare, electrice, in impuls , Brevet OSIM nr.118687 / 2003

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